In the Claims:

Further, please add claims 23-26 as indicated in the following list of claims for the present application.

1-20. (Cancelled)

21. (Previously Presented) An integrated circuit having a surface including at least one node through which the integrated circuit communicates via a signal, the integrated circuit tested by a method comprising the steps of:

a. contacting at least one node with a probe;

b. linking a terminal of an integrated circuit tester to the probe through a conductive path, such that the at least one node, the probe, the conductive path and the terminal form a signal path for conveying the signal between the integrated circuit and the integrated circuit tester,

wherein the at least one node, the probe, the terminal and the conductive path have impedances, and

wherein impedances of the at least one node, the probe, the terminal and the conductive path are sized relative to impedances of others of the node, the probe, the terminal and the conductive path to substantially optimize a frequency response characteristic of the signal path.

22. (Previously Presented) The integrated circuit of claim 1, wherein the method further comprises the impedances including inductances in series with the signal path and capacitances shunting the signal path.

23. (New) A method for sizing impedances of components in a conductive path connecting a probe of an integrated circuit (IC) test device to a terminal of an IC tester, the method comprising the steps of:

defining a frequency response characteristic desired for the conductive path;

defining attainable impedance value ranges for the components of the conductive path; and

determining a combination of impedance values for the components of the conductive path within the defined frequency response characteristic.

24. (New) The method of claim 23, wherein the components of the conductive path further comprise:

a printed circuit board (PCB) including first conductors forming a first part of said conductive path for connecting to the terminal of the IC tester;

a space transformer including second conductors forming a second part of said conductive path connecting to the probe; and

an interposer including third conductors for conveying signals between said first and second conductors.

25. (New) The method of claim 23, wherein the combination of impedance values determined provides an optimum frequency response characteristic within limits of the desired frequency response characteristic.

26. (New) A processor readable medium storing code, the code when executed performing the steps of claim 23.